REMARKS

Dear Sir:

This is a Response to the Office Action in the above referenced application mailed on October 6, 2005, and for which a 3-month extension is hereby requested. To present a more focused response, the previously pending method claims (27-35, 37-50, 54, 55, 63, and 64) have been cancelled and will be pursued separately, leaving only the device claims. Of the device claims, independent claims 3 and 15 have been amended to more clearly delineate their distinction over the prior art, with dependent claim 12 being cancelled. Pending claims 3-11 and 15-25 were rejected either under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al. or under 35 U.S.C. 103(a) with Peyret at the primary reference, with claims 15 and 22 also rejected under 35 U.S.C. 103(a) with US patent number 5,995,018 of Hane et al. as the primary reference. As described below under the corresponding headings, it is respectfully submitted that all of these rejections are in error.

Claim Objections

The Office Action objected to claims 3-11 and 15-25 due to the limitation of "a mass storage memory", which it finds to be an informality, stating "It is unclear at what point the size of a memory becomes a mass storage memory." It is respectfully that "mass storage memory" is not an informality, but is rather a term that would be understood in the art. Further, it is respectfully submitted that the Office Action is being inconsistent in making this objection: although the Office Action finds "mass storage memory" to be an informality in paragraph 71 on page 25, on page 27 in paragraph 76 in the "Response to Arguments" section it cites Wikipedia article on "Mass Storage" to the effect that it is a term of art.

As to the application itself, the Office Action is correct in so far as the Application does not contain an explicit statement of a specific point for which memory becomes "mass memory" (such as "a capacity in excess of *x* Megabytes"); however, such memories are known in the prior and discussed in the Background section of the present application, such as the familiar sort prior art memory cards that are known in the art (compact flash/MMC/SD) on which the invention is based. Reference is made to the discussion of Figure 1 given in paragraphs [0014]-[0016].

More specifically, the present invention builds on the sort mass storage memory cards known

in the prior art by adding on the sort of processing capabilities described in the application. Examples of cards having mass storage memory are discussed in the Background section, including cards such as the compact flash card (described in paragraph [0006]) and MMC and SD cards (described in paragraph [0009]). These memory cards are designed for bulk storage of user data. These are distinguished from cards such as the smart cards or SIM cards (paragraphs [0010] and [0011]), which have low memory capacities and not meant to have storage of user data. (In fact, a basic concept of the smart card is to protect the memory contents so that the user is *unable* to access its comments.) In terms of capacity, at the time of the application, examples of such memory cards had capacities on the order of several hundred Megabytes, as is described for the compact flash card in paragraph [0006].

An example of mass storage memory is perhaps most fully described in paragraphs [0014]-[0016] of the Background section in terms of the sort of memory card that the present invention builds upon. To some extent, in this context a "mass storage memory" can be characterized by the last sentence of paragraph [0015]: "The contents in the mass storage memory 111 can not be addressed randomly by the controller 131, or, more accurately, can only be accessible in blocks that are too large for the controller to utilize without first reading out and caching the whole block."

Rejections based on Peyret et al.

The Office Action rejected claims 3-11 and 15-25 were rejected either under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al. or under 35 U.S.C. 103(a) with Peyret at the primary reference. The Peyret reference presents a smart card. An important aspect of a smart card is that the contents, whether applications or data, are protected so as to not be accessible to a user. There may data related to a user, but this is host-cart system data, not user data, and is protected precisely in order to prevent user access. The Peyret reference describes some improvements to the basic smart card, but still operates fully within the smart card concept. Peyret includes a non-volatile memory to which applets can be added, but these require a special host to add (a "universal loader 62") and are host-card system applets and are again protected *from* the user's access. This ability to load applets while being able to protect them *from* the user appears to be the whole point of the Peyret reference, as described, for example, at column 5, lines 13-35. These applications may then operate on data, but this data is also system data protected *from* a user

of the card. The user of the non-volatile memory NVM in Peyret is introduced to be able to store these protected applets, as described at column 5, lines 7-9: "The NVM may preferably be used to store one or more applications which may be referred to as applets *due to the small size* of the actual program code." As the added emphasis indicates, what is being stored in Peyret's NVM is of limited size, for both the applications and any system data.

In contrast, according to aspects to which the currently pending claims are drawn, the present invention incorporates a user data portion as part a mass storage memory, allowing the user to store and access data and also process this user data as it is transferred between the card and a host. Further, these applications for use on the user data can be stored also are stored in the mass storage memory.

In its Response to Arguments section that begins on page 26, the Office Action made several comments (in paragraphs 74-76) that relate to the rejections based on Peyret. In paragraph 74, the Office Action states: Applicant has argued that flash memory is not accessed in a non-linear manner. In response, the Examiner notes that the most common type of flash memory has an I/O interface which allows only sequential access to data, as evidenced by the Wikipedia article ... and the Embedded Control Europe Article". It is respectfully submitted that these comments are inaccurate or improper on several accounts. First, it is noted that both of these cited reference are from after the filling date of the present application and are, therefore, being improperly used.

Secondly, the claim limitation in question is "wherein the mass storage interface is a non-linear interface", whereas the cited portions of these article do not relate to the memory interface but, rather, to the *architecture* of memory arrays, something on which the claims are silent. Specifically, the cited portions of both articles relate to the differences between a NOR-type array architecture and a NAND-type array architecture. In a NOR-type array, any memory cell can be directly accessed by the intersection of the bit line and word line at whose intersection the cell is formed. In contrast, in a NAND-type array, memory cells are formed into strings of memory cells arranged in series between select transistors. To access a given cell in a NAND array requires the whole string to be accessed. It is this *physical* structure of the *memory array* to which the cited portions of these articles are referring, and not the interface by which the memory accessed.

Further, it is respectfully submitted that the comments of the previous Amendment are being mischaracterized: It was not "argued that flash memory is not accessed in a non-linear manner", as a

flash memory may very well be accessed in this manner. Rather, the point (or at least the intended point) was that "flash" describes how the memory erased, not how it is accessed.

Finally, as to what is meant by "a non-linear interface", it is believed that this term is not indefinite, but is sufficiently developed in the specification. For example, see the last portion of paragraph [0015]:

> The mass storage interface 115 serves as a "non-linear" or "non-random" access interface for controlling the FLASH memory where data is stored in a non-linear fashion. The contents in the mass storage memory 111 can not be addressed randomly by the controller 131, or, more accurately, can only be accessible in blocks that are too large for the controller to utilize without first reading out and caching the whole block.

Concerning the comments in paragraph 75, it not believed that the comments are well-founded or accurate; however, in order to facilitate the application process, claims 3 and 15 have been amended to read "a card bus *to which* the processing unit, the interface and the program storage memory are connected", where, as the added emphasis indicates, the claims now explicitly states that these elements are connected to the card bus. As for the comment "nor do [the claim limitations] preclude the bus from being comprised of multiple sub-buses, the claim states that these particular elements are connect to "***a*** card bus", where as the added emphasis indicates, these elements are connected to the same, single bus.

In paragraph 76, the Office Action states "the Examiner notes that a flash memory is a type of mass storage memory" and cites a Wikipedia article on "Mass storage". This is respectfully submitted to be inaccurate: although flash memory can be used in mass storage applications, flash memory need not be a mass storage memory. Flash memory is defined by the manner in which it is *erased*, namely that cells are erased in groups (an erase block), and not to how it is *accessed* or its *size*. In various implementations, an erase block may the size of a sector or smaller and a "flash memory" need not be a mass storage memory. (Concerning the comment that "It is unclear as to at what point the size of a memory becomes a mass storage memory", this has been discussed above with respect to the claims objections.) Additionally, it is again noted that date of the cited Wikipedia article is from July 2005, long after the filing date of the present application, and is consequently being improperly cited.

Claims 3-11

Turning to the claims themselves, claims 4-11 are dependent claims having claim 3 as their

base claim. The Office Action rejected these either under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al., or under 35 U.S.C. 103(a) with Peyret as the primary reference. It is respectfully submitted that this rejection is in error.

Claim 3 reads:

> An add-on card for detachably coupling to a processing system comprising:
> an interface for communicating with said processing system while said add-on card is coupled with said processing system;
> a program storage memory storing at least one operating sequence;
> a mass storage memory including a portion for storing user data and a program memory portion storing at least one additional operating sequence;
> a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processing unit can operate on user data transferred between the mass storage memory and the processing system through the interface according to said at least one additional operating sequence;
> a card bus to which the processing unit, the interface and the program storage memory are connected; and
> a mass storage interface by which the mass storage memory is connected to the card bus, wherein the mass storage interface is a non-linear interface.

This includes a number of elements not found in Peyret.

More specifically, the claim recites "a *mass storage memory* including a portion for storing *user data*", where the emphasis has been added and the claim has been amended to make it explicit that the mass storage memory has a user data portion. As discussed above, all the teaching of Peyret are within the context of a smart card where it is important to protect the content *from* the user. Peyret neither teaches nor suggests storing user data. In its rejection of claim 12 (which, being largely redundant, has now been cancelled), the Office Action cites Peyret at column 7, lines 33-67, for disclosing user data; however, it is respectfully submitted that what is being described there is not user data. Rather, this passage describes the loading by the system of an applet from a special host (loader 62) to the card and how this is protected so that a user is *unable* to access, thus maintaining the associated rights and security. There is no disclosure of a user being able to store on the card in the memory the user's own data.

Additionally, as already discussed some above, Peyret does not disclose "a mass storage memory". The Office Action cites Figure 1 and column 5, lines 7-11, but this only refers to the storing of applets in a NVM 30. (It should also again be noted that these are applets, which specifically are applications of quite limited size.) However, the structure Peyret is that of a Smart Card, which, as discussed above and at paragraph [0010] of the present application, lacks "a mass

storage memory"; rather, the use of such a mass storage memory would be contrary to the purposes of such a smart card. There is disclosure that NVM 30 may be flash, but as discussed above, this is not the same as a mass storage memory. As far as can be determined, Peyret neither teaches nor suggests the inclusion of a mass storage memory: the discussion in terms of applets rather suggests the opposite. Thus, there is not disclosure of "a *mass storage memory* including a portion for storing user data and a program memory portion storing at least one additional operating sequence", where the emphasis is added.

Claim 3 further recites, in its current form, a "processing unit [that] can operate on *user* data transferred between the mass storage memory and the processing system through the interface according to said at least one additional operating sequence". Not only does Peyret not disclose operating on user data in this manner as it is transferred between the memory and the interface, Peyret does not store any user data in the memory, as described in the preceding paragraph.

Concerning the limitation of "a card bus to which the processing unit, the interface and the program storage memory are connected", the Office Action references Figure 1 of Peyret. As already discussed further above, claim 3 is amended to that theses elements are connected "to" the bus. Figure 1 of Peyret shows CPU 22 connected to I/O 32 on one side, while on the *opposite* side on a *different* connection CPU 22 connects to the memory 24. Peyret does not disclose "***a card bus*** whereby the processing unit, the interface and the program storage memory are connected". As the added emphasis indicates, Peyret does not disclose that the elements that the Office Action identifies as the "processing unit", the "interface" and the "program storage memory" are connected along the *same* card bus; rather, distinct buses are indicated between the "processing unit" and the "interface" and between the "processing unit" and the "program storage memory".

Claim 3 also recites the limitation of "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*", where the emphasis has been added. With respect to this limitation, the Office Action states "Peyret further discloses that the mass storage is a flash memory (See Column 4 lines 63-67) which is a non-linear memory. Thus, the mass storage interface is inherently a non-linear interface." As discussed in more detail above, Peyret does disclose a flash memory, but otherwise the Office Action is making improper and incorrect assumptions. In particular, the term "flash" in "flash memory" refers to the manner in which the memory is *erased*, namely that cells are erased in groups (an erase block), and

not to how it is *accessed*. In particular, in its discussion of Figure 3 beginning on line 1 of column 6 where Peyret discusses the memory of a smart card and its being organized into an operating system layer, this would be indicative of a random access memory structure, rather than a non-linear interface structure. This distinction is structure is discussed in the present application as presented at, for example, the last two sentences of paragraph [0015] or paragraph [0032]. As far as can be determined, Peyret neither teaches nor suggests "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*".

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 3 and dependent claims 4-11 under U.S.C. 102(b) as anticipated by Peyret is not well founded and should be withdrawn.

Many of dependent claims 4-11 are believed further allowable for the various additional limitations that they recite.

Concerning claim 4, the Office Action states that "data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion"; however, claim 4 *does not say* that the data is "transferred in streaming fashion". What the claim *does* say is "wherein the data transferred between the card and the processing system is ***continuous media***", where the emphasis is added. Peyret has no disclosure of "continuous media", which is described, for example, in paragraphs [0036] or [0043] of the present application. Continuous media encompasses data which is presented to a user in a continuous manner, such as video or audio, rather than, say a photo:

> For example, as discussed below, this arrangement allows continuous media, such as audio, video, or other streamable content, to be stored in compressed form on the card along with decompression capability lacking in the host, so the continuous media can be supplied to the host in decompressed form. In addition to continuous media, other examples of compressed data may include other large data files, for example a high-resolution X-ray. [last portion of paragraph [0036]]

Consequently, claim 4 and its dependent claim, claim 5, are believed further allowable on this basis.

Concerning claim 8, any decryption or encryption routines disclosed in Peyret are not for use on user data, but rather on *system* data to protect it *from* the user.

Similarly, as recited in claims 6, 7, and 9, these are all operating sequences that would be executed on user data transferred between the memory and the host interface. Peyret lacks use data and only discloses operations on system data.

Claims 15-25

Claims 16-25 are dependent claims having claim 15 as their base claim. The Office Action rejected these either under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al., or under 35 U.S.C. 103(a) with Peyret as the primary reference. It is respectfully submitted that this rejection is in error.

Claim 15 reads:

> An add-on card for detachably coupling to a processing system comprising:
> an interface for communicating with said processing system while said add-on card is coupled with said processing system;
> a program storage memory storing an operating sequence;
> a processing unit coupled to said interface and said program storage memory;
> a ***mass storage memory including a portion for storing user data*** coupled to said processing unit, whereby the processing unit can operate on ***user data*** transferred between the interface and the portion of the mass storage memory for storing user data according to said operating sequence;
> ***a card bus to which*** the processing unit, the interface and the program storage memory are connected; and
> a mass storage interface by which the mass storage memory is connected to the card bus, ***wherein the mass storage interface is a non-linear interface.***

As the added emphasis indicates, claim 15 contains many of the same elements as (and has been amended similarly to) claim 3. Consequently, it is believed allowable for the reasons given above with respect to claim 3.

More specifically, claim 3 includes "a mass storage memory", where this memory "include[es] a portion for storing user data", "operate[s] on user data transferred between the interface and the portion of the mass storage memory", includes "a card bus to which the processing unit, the interface and the program storage memory are connected", and has a "mass storage interface [that] is a non-linear interface". As discussed above with respect to claim 3, none of these features are disclosed by Peyret. Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 15 and dependent claims 16-25 under U.S.C. 102(b) as anticipated by Peyret is not well founded and should be withdrawn.

Many of dependent claims 16-25 are believed further allowable for the various additional limitations that they recite. In particular, the further limitation of claims 17-19 is discussed above with respect to claim 4 and believed further allowable on this basis. Similar, claims 23, 20, 21, and 24 are believed allowable for reasons discussed above with respect to claims 8, 6, 7, and 9, respectively, above.

Rejections based on Han et al.

The Office Action also rejected independent claim 15 under 35 U.S.C. 103(a) as being unpatentable over US patent number 5,995,018 of Hane et al. in view of FOLDOC. It is respectfully submitted that this rejection is also in error.

The Hane reference describes an information transfer system that includes an IC card that basically functions as an advanced form of ticket. This ticket 1 is shown to interact with a couple of different hosts, but the structure of the ticket 1 is shown in Figures 1, 2, and 6, with the device in Figure 6 differing only in that it also includes a display section 29 that does not enter into the discussion here. Hane's ticket 1, as described beginning on line 15 of column 3, is shown to include an Antenna 8 and "a modulation/demodulation circuit 9", which receive a signal from a host and present it to the controller 10; that is, these elements together act as a host interface, performing the minimal function to data so that data can be communicated with a host. Further, the "modulation/demodulation circuit" is a *circuit* and, as such, is hardware; there no discussion of it operating on the data according to an operating sequence stored in a memory. (Hane has no disclosure of a program storage memory, the only memory being Memory 11, of which there is no disclosure of it storing any operating sequences.) Hane's ticket 1 also includes a controller 10; however, Hane provides no disclosure of what this controller actually does. Hane neither teaches nor suggests that this controller 10 does anything beyond any sort of minimal management that would qualify it for the term of "controller": in particular, Hane provides no teaching that this controller 10 performs any sort of processing on user data, whether by according to an operating sequence or otherwise. As for Hane's memory, this is described with the primary function of storing the system information needed for automated ticket-checking (see, e.g. beginning at line 66 of column 4) and also for "additional information". The ticket 1 receives this "additional information", stores it in memory 11, and provides it back: there is no disclosure it being operated on in anyway, and in particular not being operated on by a processing unit (which Hane lacks) using an operating sequence stored in a program storage memory (which Hane also lacks).

As for claim 15, this recites:

> An add-on card for detachably coupling to a processing system comprising:
> an interface for communicating with said processing system while said add-on card is coupled with said processing system;
> a program storage memory storing an operating sequence;
> a processing unit coupled to said interface and said program storage memory;

a mass storage memory including a portion for storing user data coupled to said processing unit, whereby the processing unit can operate on user data transferred between the interface and the portion of the mass storage memory for storing user data according to said operating sequence;

a card bus to which the processing unit, the interface and the program storage memory are connected; and

a mass storage interface by which the mass storage memory is connected to the card bus, wherein the mass storage interface is a non-linear interface.

It is respectfully submitted that this contains a number of elements neither found in, nor suggested by, Hane or FOLDOC, either alone or in combination.

Concerning "a program storage memory storing an operating sequence", such a memory is not found in Hane and the Office Action provides not indication that it does. The Office Action does state that Hane has "a processing unit which includes a program storage memory storing an operating sequence (See Figure 1 Numbers 10 and 11)". This is incorrect on several counts. First, the cited elements of Hane are its controller 10 and memory 11. As described in the next paragraph, Hane has no disclosure of the controller 10 have any processor capabilities. Further, as for the memory 11, the Office Action is being inconsistent, as it later seems to identify it with the "mass storage memory" of the claims. In any case, Hane has no disclosure of any storage of an operating sequence, particular Hane has no disclosure of a processing unit using such an operating sequence to operate on use data. Consequently, Hane has no disclosure of "a program storage memory storing an operating sequence".

As for "a processing unit coupled to said interface and said program storage memory", the Office Action this with the controller 10. As discussed above, Hane provides no disclosure of what this controller actually does. Hane neither teaches nor suggests that this controller 10 does anything beyond any sort of minimal management that would qualify it for the term of "controller". Specifically, there is no disclosure of it performing as a processing unit.

For "mass storage memory", the Office Action cites Hane's memory 11, which it has already previously identified with the "program storage memory". Hane has no disclosure of the memory being a "mass storage memory" and the Office Action provides no citation to this effect.

For the limitation of "the processing unit can operate on user data transferred between the interface and the portion of the mass storage memory for storing user data according to said operating sequence", the Office Action cites Column 3 lines 32-33. However, this passage only refers to the demodulation performed by the *modulation/demodulation circuit* 9, not to any

processing by the controller 10, which is the element identified by Office Action as the processing unit. Further, this modulation/demodulation circuit 9 is a *circuit*, a piece of hardware. There is no disclosure that it performs any processing "according to said operating sequence". Further there is no disclosure that it does so according to an operating sequence stored in "a program memory" (of which Hane has no disclosure). Hane only discloses storing system data ("that required for automated ticket-checking") and "additional data", where there is no disclosure of doing anything beyond simply storing this "additional data".

Concerning "a card bus to which the processing unit, the interface and the program storage memory are connected", the Office Action cites Hanes Figure 1. Figure 1 shows neither "processing unit" nor "program storage memory". As already noted, the elements of Hane that the Office Action identifies with these claim elements (controller 10 and memory 11) do not fit the requirements of the claim. Further, even accepting the Office Action's identifications, the identified elements are not connected to "***a*** bus", where the emphasis is added, but rather by a number of separate connections.

As for "mass storage interface [that] is a non-linear interface", the Office Action only cites Figure 1. However, neither in Figure 1 nor elsewhere does Hane have any disclosure of a memory interface; more specifically, Hane neither teaches nor suggests the use of a *non-linear* memory interface.

Concerning the use of the FOLDOC reference, the Office Action seems to be making the implicit argument that having EEPROM means it would be obvious to instead incorporate flash memory; and that having flash, this means both mass storage and a non-linear interface. The Office Action is correct in that Hane discloses EEPROM memory, but there is no disclosure that this is either "mass storage memory" or that it is accessed by a non-linear interface. The Office Action cites the FOLDOC article for the use of Flash memory. As already discussed above with respect to the Peyret reference, although Flash may be used for mass storage and may be accessed by a non-linear interface, neither of these need be so. What defines flash memory is how it is erased, as is supported by the FOLDOC article (where the emphasis is added): "A kind of non-volatile storage device similar to EEPROM, *but where erasing can only be done in blocks or the entire chip.*" Flash is not defined by its size nor by how it is accessed.

As for the implicit argument that having EEPROM means it would be obvious to instead incorporate flash memory, this is also believed to be incorrect. As noted in the quote from FOLDOC

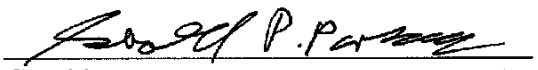
above, the advantage of flash memory is the ability to perform erasing at the block or chip level. However, the main function Hane's device is as a commuter pass or ticket, an application where small amounts of data would be rewritten frequently, something that would be contrary to a require (which is the case for flash) that the memory needs to be erased on the block or chip level every time it is rewritten. Hane recites (column 3, lines 20-22) that the "memory 11 is, for example, a ferroelectric memory of an electrically erasable and programmable read only memory (EEPROM)", both types of memory that, unlike flash, allow for easy rewriting of small amounts of data. Flash was certainly known at the time of the Hane patent, yet was not included among the suggested types of memory.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 15 and dependent claim 22 as being unpatentable over US patent number 5,995,018 of Hane et al. in view of FOLDOC is not well founded and should be withdrawn.

Conclusion

For the reasons given above, it is therefore respectfully submitted that the rejection of claims 3-11 and 15-25 are not well founded and should be withdrawn. Reconsideration of these claims and an early indication of the allowance of the present application are earnestly solicited.

Respectfully submitted,



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